REMARKS

Prior to this Amendment, Claims 1-35, including independent claims 1, 13, 17, 28, 32 and 35, were pending in the Application. Claims 1-3, 11-18, 28-32, 34 and 35 have been rejected. However, as Applicants note with appreciation, the Examiner has indicated that claims 4-10 and 19-27 have been objected to but would be allowed if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4-12, 19-25 and new claims 36-45

Claims 4, 11, 19 and 26 have been rewritten in independent form including all of the limitations of their respective base claims, as well as the non-substantive corrective amendments made to the base claims, *i.e.*, Claims 1 and 17, discussed below. Claims 4, 19 and 26, which the Examiner objected to, should now be allowable. Allowance of dependent Claims 5-10, 20-25 and 27 should follow.

New claims 36-39 correspond respectively to Claims 2, 3, 11 and 12, but depend from base Claim 4. Their allowance should therefore follow from Claim 4 as amended. Similarly, new claims 40-42 correspond respectively to claims 18, 26 and 27, but depend from base Claim 19. Their allowance should therefore follow from Claim 19 as amended. New Claim 45 corresponds to Claim 18 as filed, but depends from amended Claim 26. Allowance of new Claim 45 should follow from Claim 26, and is respectfully requested.

Although Claim 11 as filed was rejected, Applicant believes this rejection was inadvertent, because 1) in rejecting Claim 11 along with Claim 1, the Examiner did not discuss the limitation of Claim 11 as filed, namely a combiner which combines two input signals to produce an error signal; and 2) Claim 11 closely parallels method Claim 26, which the Examiner stated was allowable (see Office Action, page 4). See Office Action, page 2.

Therefore, like Claim 26, Claim 11 has been rewritten to include the limitations of its base claim, *i.e.*, Claim 1. Allowance of Claim 11, as well as dependent Claim 12 and new dependent Claims 43 and 44 (corresponding to Claims 2 and 3) is respectfully requested.

Claim rejections - 35 U.S.C. §102(e)

Claims 1-3, 11, 17, 18, 32 and 34 have been rejected under 35 U.S.C. 102(e) as being anticipated by Wei et al., U.S. Patent No. 6,369,660.

A Declaration Under 37 C.F.R. §1.131 by the inventor is being submitted concurrently with this Amendment. This Declaration, along with its accompanying exhibits, establishes a reduction to practice of the claimed invention at least as early as January 8, 1999, well before the filing date (October 27, 1999) of the Wei reference.

In view of this Declaration, Applicant respectfully requests the reconsideration and withdrawal of the rejection of Claims 1-3, 11, 17, 18, 32 and 34, in favor of allowance.

Although Applicant believes Wei is removed as prior art by the above-described Declaration, Applicant wishes to distinguish the claimed invention from Wei by pointing out that, unlike Applicant's invention which is intended to bring a VCO up to speed rapidly, Wei addresses the different problem of runaway in a phase lock loop. Wei examines the output of a VCO directly or through a divider, and limits the control signal to the VCO in order to limit the VCO output frequency. Wei does not need to, and hence does not, examine an error signal which is indicative of the difference between the VCO output frequency and a reference clock.

Applicant's frequency monitor invention, on the other hand, as recited in independent Claims 1, 17 and 32, processes an error signal whose frequency is responsive to the difference between frequencies of two input signals, for example, a VCO output signal and a reference clock, and provides an output that indicates whether this difference is within a specified range. Thus, Applicant's invention, unlike Wei, can be used to maintain the frequency of a VCO output signal within a certain range of a reference clock, by using the output of Applicant's frequency monitor to control the VCO.

Wei does not teach or suggest generating an error signal or an output indicative of the difference between frequencies of two input signals, as recited in amended Claims 1, 17 and 32. Therefore, Claims 1, 17 and 32 as amended, as well as their respective dependent claims, should be allowable even if the above Declaration were rejected.

Note that Claims 1 and 2 have both been amended to correctly refer to the antecedent "conductive circuit". Independent method Claim 17 has been amended to correct an error of grammatical nature.

Claim rejections - 35 U.S.C. §102(b)

Claims 13-16, 28-31 and 35 have been rejected under 35 U.S.C. 102(b) as being anticipated by Rizzo, U.S. Patent No. 4,787,097.

Rizzo teaches circuitry for determining when the output of a phase-locked loop (PLL) circuit is outside a narrow frequency window, and for rapidly bringing the VCO contained therein up to a frequency at which phase lock may be maintained. When the PLL is operating outside the window, a phase detector is turned off and effectively replaced with a phase frequency detector.

However, with reference to Rizzo, Fig. 3, the phase detector 12 taught by Rizzo produces a DC voltage which is proportional to the difference in frequency of the input data and the VCO output, and is not directly usable by the frequency monitor circuit 20. Rizzo requires extra circuitry 21, 23, 24 to produce an oscillating signal, whose frequency is the difference between the VCO and a reference frequency, that can be compared with the clock reference by a phase frequency detector 27.

On the other hand, Applicant's Claim 13 as amended recites the frequency lock system embodied in Applicant's Fig. 6, as described at page 8, lines 6-16 of the Specification as filed. In this embodiment, an analog data phase detector, such as that described in U.S. Application S/N 09/862,384, is employed. The output of such a detector indicates the frequency difference between a reference clock and incoming data, and can be used directly by the frequency monitor to select an oscillator's control signal, simplifying the circuit design as compared with Rizzo.

Claim 13 has further been amended to recite the frequency monitor of Claim 14, now canceled. Finally, Claim 13 has also been amended to use more definitive language than the "either ... or" language originally used.

Rizzo does not teach or suggest a frequency lock system having an analog data phase detector circuit which produces a phase detector output signal that oscillates at a frequency responsive to the difference between the oscillator output signal's frequency and an input stream's data frequency; nor does Rizzo teach or suggest a frequency monitor which controls the selector based on the frequency of the phase detector output signal, as now recited in Claim 13.

Therefore, Claim 13 should now be allowable. Allowance of dependent Claims 15 and 16 should follow.

Independent method Claims 28 and 35 have been amended similarly and should now be allowable. Claim 29, now incorporated into Claim 28, is canceled. Allowance of dependent Claims 30 and 31, amended to depend from Claim 28, should follow.

Specification

The Specification has been amended on page 8 to remove an unused reference number. No new matter has been introduced by this or any other amendments to the Application.

CONCLUSION

In view of the above amendments and remarks, it is believed that all pending claims, *i.e.*, Claims 1-13, 15-28 and 30-45, are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,

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MARKED UP VERSION OF AMENDMENTS

Specification Amendments Under 37 C.F.R. § 1.121(b)(1)(iii)

Replace the paragraph at page 8, lines 13 through 16 with the below paragraph marked up by way of bracketing and underlining to show the changes relative to the previous version of the paragraph.

During cycle-slipping, sweeping of the VCO clock phases over the data stream causes the phase detector output V_{er} [16] to oscillate between "early" and "late" signals. The frequency of this oscillation (sweep speed) is equal to the frequency difference between the receive clock and the incoming data.

Claim Amendments Under 37 C.F.R. § 1.121(c)(1)(ii)

1. (Amended) A frequency monitor, comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the [resistive] conductive circuit; and

an indicator circuit which produces an output responsive to the charge held by the capacitor.

2. (Amended) The frequency monitor of Claim 1, wherein the [resistive] conductive circuit comprises:

a switched capacitor circuit which charges and discharges at a rate that depends on the rate of the edge detector output pulses.

4. (Amended) [The] A frequency monitor, [of Claim 1, further] comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit;

an indicator circuit which produces an output responsive to the charge held by the capacitor; and

a selector which, responsive to the indicator circuit output, selects from plural sources to control an oscillator.

11. (Amended) [The] A frequency monitor, [of Claim 1, further] comprising:

a combiner circuit which combines two input signals to produce an error signal, the error signal having a frequency responsive to a difference between frequencies of the two input signals;

an edge detector which produces an output comprising a pulse for each rising/falling edge of the error signal;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit;

an indicator circuit which produces an output responsive to the charge held by the capacitor.

13. (Amended) A frequency lock system, comprising:

an oscillator which produces an output signal whose frequency is responsive to a control signal;

a frequency detector circuit which produces a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

an analog data [a data recovery] phase detector circuit which produces a phase detector output signal that oscillates at a frequency responsive to the difference between [based on] the oscillator output signal's frequency and an input stream's data frequency; [and]

a selector which selects one of [either] the frequency detector output signal [or] and the phase detector output signal as the control signal; and

a frequency monitor which controls the selector based on the frequency of the phase detector output signal.

17. (Amended) A method for monitoring frequency, comprising:

producing an output comprising a pulse for each rising/falling edge of the error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

charging a capacitor to a charge responsive to the error signal frequency; and

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount.

19. (Amended) [The] A method for monitoring frequency, [of Claim 17, further] comprising:

producing an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

charging a capacitor to a charge responsive to the error signal frequency;

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount; and

selecting, responsive to the step of indicating, from plural sources to control an oscillator.

26. (Amended) [The] A method for monitoring frequency, [of Claim 17, further] comprising:

combining [the] two input signals to produce [the] an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

producing an output comprising a pulse for each rising/falling edge of the error signal;

charging a capacitor to a charge responsive to the error signal frequency;

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount.

28. (Amended) A frequency lock method, comprising:

producing, from an oscillator, an output signal whose frequency is responsive to a control signal;

producing, from a frequency detector circuit, a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

producing, from [a data recovery] an analog phase detector circuit, a phase detector output signal that oscillates at a frequency responsive to the difference between [based on] the oscillator output signal's frequency and an input stream's data frequency; [and]

selecting one of [either] the frequency detector output signal [or] and the phase detector output signal as the control signal; and

controlling the selector with a frequency monitor.

30. (Amended) The method of [Claim 29] Claim 28, wherein the frequency monitor selects the phase detector output signal if the oscillator frequency and input data frequency are within a predetermined margin, and selects the frequency detector output signal otherwise.

31. (Amended) The method of [Claim 29] Claim 28, wherein the frequency monitor selects the phase detector output signal if the oscillator frequency and a reference clock frequency are within a predetermined margin, and selects the frequency detector output signal otherwise.

35. (Amended) A frequency lock system, comprising:

means for producing, from an oscillator, an output signal whose frequency is responsive to a control signal;

means for producing, from a frequency detector circuit, a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

means for producing, from [a data recovery] an analog data phase detector circuit, a phase detector output signal that oscillates at a frequency responsive to the difference between [based on] the oscillator output signal's frequency and an input stream's data frequency; [and]

means for selecting one of [either] the frequency detector output signal and [or] the phase detector output signal as the control signal; and

means for controlling said means for selecting based on the frequency of the phase detector output signal.